Red River

Pocket Change

Model 351

- *Fits standard PCMCIA Type II socket*
- *14-bit (80 MSPS) A/D Converter*
- *14-bit (80 MSPS) D/A Converter*
- *Internal or external sample clock*
- *Factory selectable crystal frequency*
- *Xilinx Virtex-4 LX , SX, or FX FPGA*
- *Signal capture FPGA function included*
- *Signal generator FPGA function included*
- *Verilog/VHDL interface source code*
- *PCI bus master with auto DMA features*
- *DMA scatter-gather operation*
- *Windows and Linux drivers available*

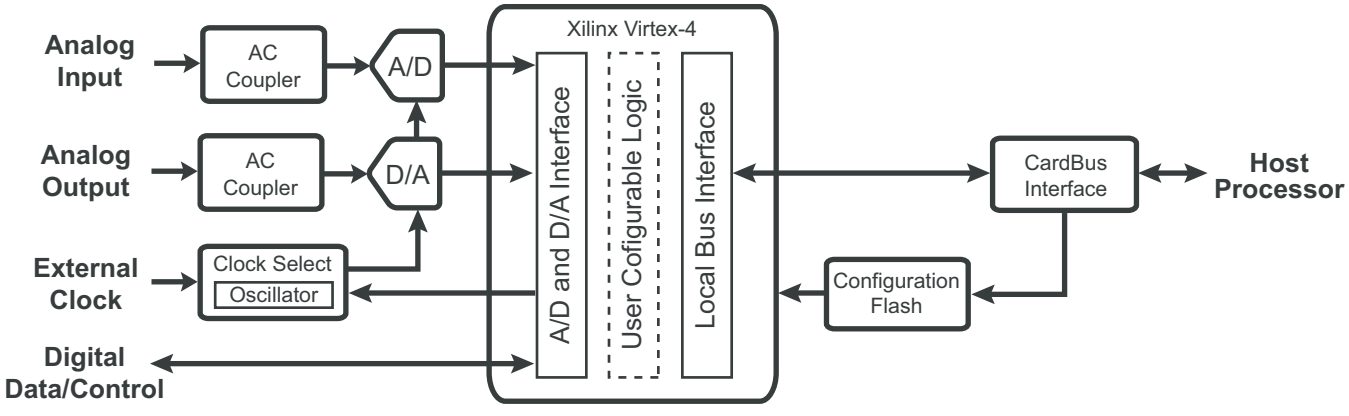
CardBus FPGA Transceiver

Pocket Change provides the ideal platform to rapidly field application specific transceiver functions minus the expense of custom hardware development. The architecture features a high performance ADC and DAC tightly coupled to a Xilinx Virtex-4 FPGA. The FPGA communicates with the host processor through a dedicated CardBus bridge, leaving the majority of the logic uncommitted. Simple interfaces to the ADC, DAC, and local bus are easily integrated with user application logic.

Pocket Change interfaces to external analog receive and transmit channels through MMCX coax connectors on the outside edge of the card. These connectors are AC coupled to a 14-bit ADC and 14-bit DAC that share a common clock. The sample clock source is software selectable from either the 80 MHz on-board crystal oscillator or an external input that is also supplied through an MMCX connector. A Digital port is available to directly connect the FPGA to external LVTTL or LVDS signals. The internal JTAG chain is also available from the digital connector for external programming and debug using the Xilinx iMPACT™ and ChipScope™ tools.

Pocket Change can be equipped with parts from all three of the Virtex-4 PFGA platforms. Devices from the high performance logic (LX) platform supply a wide range of gate densities to general purpose applications. Devices from the high-performance signal processing (SX) platform offer an abundance of dedicated DSP hardware resources for math intensive applications. The embedded processing platform (FX) option adds a PowerPC block to the FPGA fabric. Each platform offers multiple speed grades to deliver the level of performance needed to meet real-time processing demands.

Pocket Change can operate as a CardBus master or target, allowing DMA transfers to be initiated either autonomously by the transceiver or under direct control of the host. A DMA core is provided to monitor FIFO thresholds in the FPGA and signal either the local controller or the host for service. DMA scatter-gather techniques are supported by both the hardware and software to optimize data transfer efficiency.



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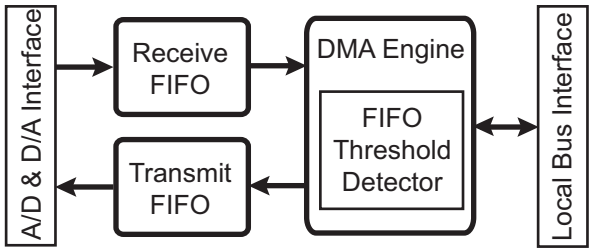

Default FPGA Configuration (Signal Acqusition/Generation)

The Virtex-4 FPGA is supported by a robust set of development tools from Xilinx. Creation of user configuration code follows the standard design flow using a pin assignment file supplied with the *Pocket Change*. Verilog and VHDL source code for the ADC, DAC, and local bus interface logic are also provided. Both the FPGA and the Configuration PROM can be programmed directly over the CardBus.

The *Pocket Change* product ships with a default configuration preloaded in the PROM to quickly establish communication with the host computer. The card will immediately function as a signal acquisition/generation unit when power is applied. Sample code is provided to collect data from the receiver channel, supply data to the transmitter channel, and demonstrate DMA operation in a loopback mode.

The signal acquisition/generation function uses the internal BlockRAM resources of the FPGA to provide FIFOs between the A/D or D/A converter and the local bus. Registers are used to set a threshold on each FIFO that will trigger a service request to the DMA engine.

The DMA engine acts as a CardBus master to initiate data transfers between the FIFOs and host memory. A set of source/destination addresses, DMA block size, and DMA block count are preloaded by the host to manage the transaction. An interrupt is generated by the *Pocket Change* when the final block of the current count has been written.

Typical Applications

- *General purpose signal acquisition/generation*
- *Software defined radio transceiver*
- *Signal intelligence (SIGINT) collection*
- *Transceiver modem algorithm prototyping*
- *Frequency hop signal generator*
- *Portable signal recorder/playback*

Specification Summary

External Interfaces

AD9245 14-bit A/D converter
80 MSPS maximum sample rate

AD9744 14-bit D/A converter
80 MSPS maximum sample rate

Digital Port
8-bit bidirectional LVTTL or LVDS bus

FPGA

User configurable Xilinx Virtex-4 FPGA
Verilog/VHDL interface source code
Default signal acquisition/generation core
Configuration via PROM or CardBus

Board

32-bit/33 MHz CardBus PCI
Dual channel auto DMA engine
1024 DMA buffer addresses per channel

Options

XC4VLX40 -11, or -12 Speed Grades
XC4VLX60 -11, or -12 Speed Grades
XC4VSX25 -11, or -12 Speed Grades
XC4VSX35 -11, or -12 Speed Grades
XC4VFX12 -11, or -12 Speed Grades
Selectable Oscillator Frequency

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