FPGA Configurable
Dual Channel Receiver

The Channel Express product family provides the ideal platform to rapidly field application specific signal acquisition and generation functions minus the expense of custom hardware development. All of the products share a common FPGA processing architecture and code base with different interface options tailored to a variety of market needs.
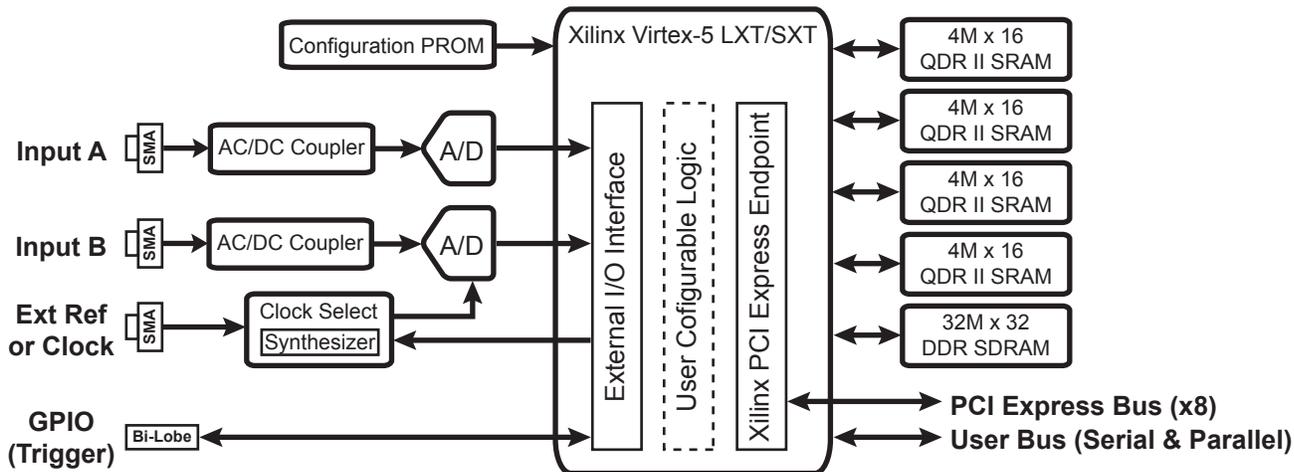
The Model 363 is designed around the Texas Instruments ADS5474 14-bit ADC. The 400 MHz sample clock is supplied by either an on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz TCXO or an external reference can be used to achieve system-wide phase coherence.

The analog ADC inputs can be either AC or DC coupled to the external environment. The AC coupled configuration supports direct IF sampling (bandpass sampling) beyond the first Nyquist zone. The DC coupled option allows operating frequencies to approach zero without attenuation.

The FPGA is selected from the Xilinx Virtex-5 high performance logic (LXT) or signal processing (SXT) platforms. A variety of size and speed grade options are offered to optimize the price/performance ratio over a wide range of applications. The FPGA communicates with the host processor through an integrated endpoint block for PCI Express, leaving the majority of logic uncommitted for customer applications.

The Model 363 includes up to 32 Mbytes of QDR SRAM and 128 Mbytes of DDR SDRAM. The QDR SRAM interfaces to the FPGA through separate 16-bit read and write ports to achieve a combined 8 Gbytes/sec data transfer rate. This allows high-speed signal acquisition or generation independent of PCIe bus throughput. A 32-bit DDR SDRAM is available to meet lower rate, high-capacity storage needs.

The Model 363 is available as a PCI Express mezzanine card (XMC.3) or half length PCI Express adapter card. Both form factors offer eight lane (x8) bus operation and support

- ▲ **Available in XMC and PCIe form factors**
- ▲ **Dual 14-bit analog-to-digital converter (ADC)**
- ▲ **50 to 400 MHz sample clock frequency**
- ▲ **AC or DC coupled analog inputs**
- ▲ **Xilinx Virtex-5 LXT or SXT FPGA**
- ▲ **32 Mbytes SRAM / 128 Mbytes SDRAM**
- ▲ **On-board fixed frequency synthesizer**
- ▲ **FPGA core library for data interfaces**
- ▲ **PCI Express (PCIe) eight lane (x8) bus**
- ▲ **Bus master with scatter-gather DMA**
- ▲ **Windows, Linux, VxWorks drivers & API**
- ▲ **Reference design with source code**

down-shifting to four lanes (x4). Both cards also include up to eight additional user defined serial links that can be configured in the FPGA. An optional user defined parallel bus is offered for compatibility with legacy hardware.

An optional 50 ohm trigger input is available on the front of the Model 363 to synchronize data processing to an external event. It can also be used to synchronize an on-board time-of-day clock with an external GPS or IRIG timing source. Additional bidirectional general purpose I/O links are available for digital control signals.

The Virtex-5 FPGA is supported by a robust set of development tools from Xilinx. Creation of user configuration code follows the standard design flow using a pin assignment file supplied with the product. Cores are provided in VHDL source code for interfaces to the ADC, DAC, SRAM, DRAM, utility functions, and PCI Express Endpoint block.

Source code is also provided to the DMA FPGA core that manages data transfers between the Model 363 and host memory. The DMA engine allows the transceiver to automatically initiate a PCI burst transaction when data needs to be transferred. DMA chaining and scatter-gather techniques are supported by both the hardware and software to optimize data transfer efficiency using up to 2048 buffers in host memory.

The FPGA configuration PROM can be programmed from software over the PCIe host connection. A JTAG port is also available to load the PROM directly or debug application logic using Xilinx ChipScope.

The Model 363 ships with diagnostic firmware preloaded in the PROM to quickly verify hardware and software integrity when it is installed on the host computer. The diagnostic software performs a snapshot signal capture on all receiver channels simultaneously. The data from each channel is stored in a separate disk file for analysis. A verification utility is also provided to analyze the data and report the characteristics of the signal that was captured.
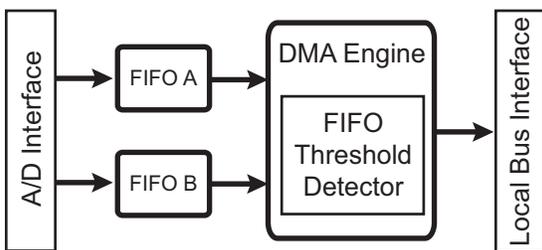
FPGA Diagnostic Function (Dual Channel Signal Acquisition)

Typical Applications

- ▲ **Multi-channel data acquisition**
- ▲ **Multi-channel software defined radio receiver**
- ▲ **Signal intelligence (SIGINT) collection**
- ▲ **Receiver algorithm prototyping**
- ▲ **Beamforming / TDOA**
- ▲ **Signal recorder**

▲ Receiver Performance

Measured characteristics*:
  3 dB passband (AC): 0.1 to 1300 MHz
  3 dB passband (DC): TBD
  SNR (AC): 70 dB (20/70/125 MHz)
  SNR (DC): TBD
  SFDR (AC): 86/84/84 dB (20/70/125 MHz)
  SFDR (DC): TBD
  Channel isolation: 85 dB (250 MHz)
Phase noise: -100 dBc/Hz (10 kHz offset)
Internal reference: 10 MHz +/- 1.5 ppm

Consult the Hardware Reference Manual for details.

▲ Hardware

Form factor: XMC.3 or half-length PCIe
PCIe Lanes: x8 or x4 (down-shift)
GPIO: 6-bit LVTTL or LVDS
Optional external reference or sample clock
External trigger input (50 ohms)
Serial User bus: Up to 8 transceiver lanes
Parallel User bus: 62-bit LVTTL or LVDS
Power dissipation: 10 to 22 Watts
Airflow: 250 LFM at 35 degrees C

▲ Software

Fedora Linux kernel 2.4 or 2.6
Windows 2000, XP, or Server
VxWorks v6 (Kontron CP6012 target)

▲ Build Options

Virtex-5 FPGA:
  LX50T-2/-3, LX85T-2/-3, LX110T-2/-3
  LX155T-2/3, SX50T-2/-3, SX95T-2
Synthesizer frequency:
  400 MHz (Maximum ADC specification)
  213 MHz (160 MHz IF sampling)
Depopulate memory for cost/power benefit
Conformal coat for harsh environments

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