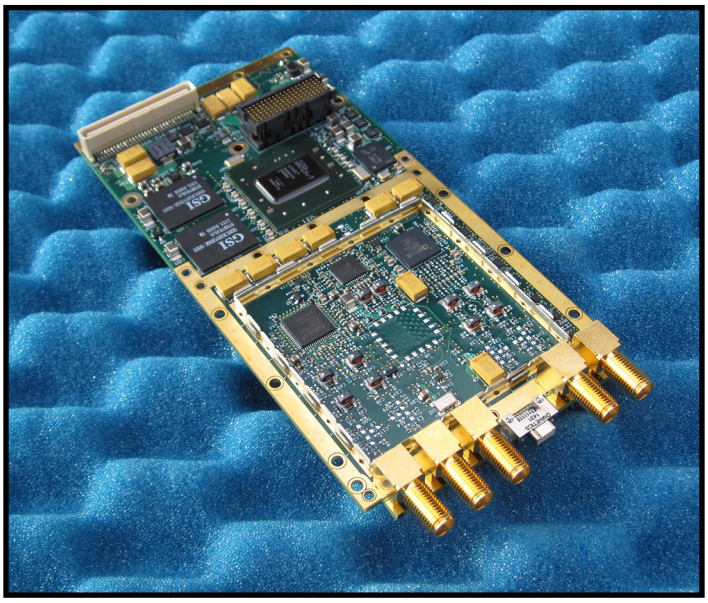
Red Rapids

SigFPGA™ XCVR2 16/310

Model 372



- **Available in XMC, CCXMC, PCIe formats**
- **Dual channel transceiver (310 MHz)**
- **16-bit AC or DC coupled ADC and DAC**
- **Three Xilinx Kintex-7 FPGA size options**
- **Two banks of QDR II+ SRAM (32 Mbytes)**
- **On-board frequency synthesizer**
- **Temperature and current monitors**
- **PCI Express (PCIe) x8 Gen 2 bus**
- **Scatter-gather DMA bus master**
- **FPGA core library for data interfaces**
- **Windows, Linux, VxWorks drivers & API**
- **Reference design with source code**

FPGA Signal Processor

The SigFPGA™ product family provides the ideal platform to rapidly field application specific signal acquisition and generation functions minus the expense of custom hardware development. All of the products share a common FPGA processing architecture and code base with different interface options tailored to a variety of market needs.

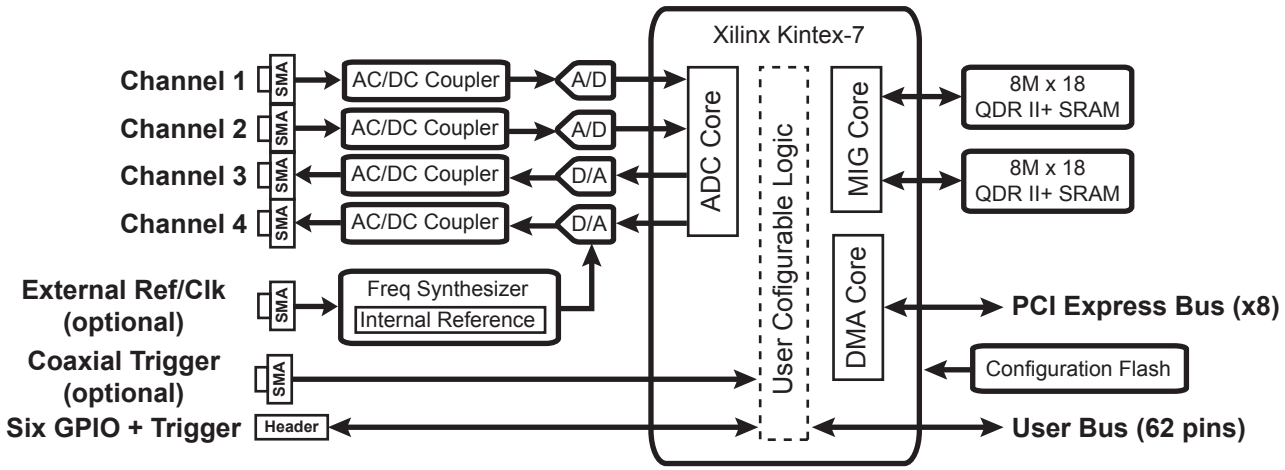
The Model 372 is designed around the Analog Devices AD9652 16-bit ADC and AD9142A 16-bit DAC. The 310 MHz sample clock is supplied by either the on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz TCXO or an external reference can be used to achieve system-wide phase coherence.

The Model 372 is available as a PCI Express mezzanine card (XMC), conduction cooled mezzanine card (CCXMC), or half-length PCI Express (PCIe) adapter card. The CCXMC can be mounted to any VITA 20-2001 compliant host without modification. All form factors offer four lane (x4) or eight lane (x8) bus operation at Gen 2 performance. An optional user defined parallel bus is also available on the XMC P4 connector or a rear facing connector on the PCIe adapter.

The FPGA is selected from the Xilinx Kintex-7 platforms. A variety of size and speed grade options are offered to optimize the price/performance ratio over a wide range of applications. The FPGA communicates with the host processor through an integrated endpoint block for PCI Express, leaving the majority of logic uncommitted for customer applications.

The Model 372 includes 32 Mbytes of QDR II+ SRAM operating at 500 MHz. The SRAM interfaces to the FPGA through separate 18-bit read and write ports to achieve a combined 8 Gbytes/sec data transfer rate. This allows high-speed signal acquisition independent of PCIe bus throughput.

A general purpose I/O (GPIO) header provides six bidirectional signals to communicate with external hardware. The GPIO header also includes a 50 ohm terminated trigger input to



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synchronize with an external event or clock source.

The GPIO header also provides the JTAG connections to the FPGA. The JTAG port is used to program the configuration flash memory or connect the Xilinx ChipScope tool for debug.

A 50 ohm terminated coaxial input offers an optional second trigger source that provides controlled impedance through the cable interconnect. The Model 372 can have either the external clock/reference input or the coaxial trigger input, but not both.

The Model 372 monitors both power consumption and temperature for ultimate visibility into the actual operating characteristics of a specific FPGA design. Current measurements are available on all of the primary voltage supplies. Temperature sensors monitor the FPGA die temperature and five other locations on the card.

The Kintex-7 FPGA is supported by a robust set of development tools from Xilinx. Creation of user configuration code follows the standard design flow. Cores are provided in VHDL source code for interfaces to the ADC, DAC and command/status utility functions. Pregenerated Xilinx Coregen functions are supplied for the SRAM interface and PCI Express Endpoint block. The EZDMA2 core from PLDA is supplied with the product in EDIF netlist format at no additional charge.

The EZDMA2 core manages data transfers between the Model 372 and host memory. The DMA engine allows the receiver to automatically initiate a PCI burst transaction when a channel requires service. High performance DMA techniques are supported by both the hardware and software to optimize data transfer efficiency. Memory fragmentation problems are eliminated by supporting thousands of scatter-gather DMA buffers in host memory.

The Signal FPGA ships with diagnostic firmware preloaded in the PROM to quickly verify hardware and software integrity when it is installed on the host computer. The diagnostic software performs a snapshot signal capture on all receiver channels simultaneously. The data from each channel is stored in a separate disk file for analysis. A verification utility is also provided to analyze the data and report the characteristics of the signal that was captured.

Typical Applications

- **Multi-channel voice/data communications**
- **Signal collection with calibration source**
- **Software defined radio**
- **Algorithm prototyping**
- **Signal recorder**

Specification Summary

Transceiver Performance

Measured characteristics:
- RX full power (3 dB) BW: 400 MHz
- RX SNR: 75 dB (First Nyquist typical)
- RX SFDR: 95 dBc (First Nyquist typical)
- TX noise spectral density: -160 dBm/Hz
- TX SFDR: 84 dBc (second harmonic)
- Channel isolation: 90 dB (typical)

Phase noise: -100 dBc/Hz (10 kHz offset)
Internal reference: 10 MHz +/- 1.0 ppm

Hardware

Format: XMC, CCXMC, half-length PCIe
PCIe: x4 or x8 Gen 2
GPIO: 6-bit LVTTL or 3-bit LVDS
Selectable internal or external sample clock
Selectable internal or external reference
External trigger input (50 ohm terminated)
User bus: 62-bit LVTTL or 24-bit LVDS
Power dissipation: 10 to 20 Watts

Software

Adapter driver: Linux, Windows, VxWorks
FastApp interpreter and C code generator
Signal Stream Lite application example

Build Options

External clk/ref OR coaxial trigger
Kintex-7 FPGA:
- XC7K160T, XC7K325T, XC7K410T

Synthesizer frequency:
- 310 MHz (Maximum ADC specification)
- 213.33 MHz (160 MHz IF sampling)
- Programmable (Degraded phase noise)

Depopulate memory for cost/power benefit

Red Rapids
797 North Grove Rd, Suite 101
Richardson, TX 75081
Phone: 972-671-9570
Fax: 972-671-9572
www.redrapids.com