# Red Rapids

## SigFPGA™ RX4 16/250
### Model 377


**PCIe**


**XMC**


**CCXMC**


**VPX**

The SigFPGA™ product family provides the ideal platform to rapidly field application specific signal acquisition and generation functions minus the expense of custom hardware development. All of the products share a common FPGA processing architecture and code base with different interface options tailored to a variety of market needs.
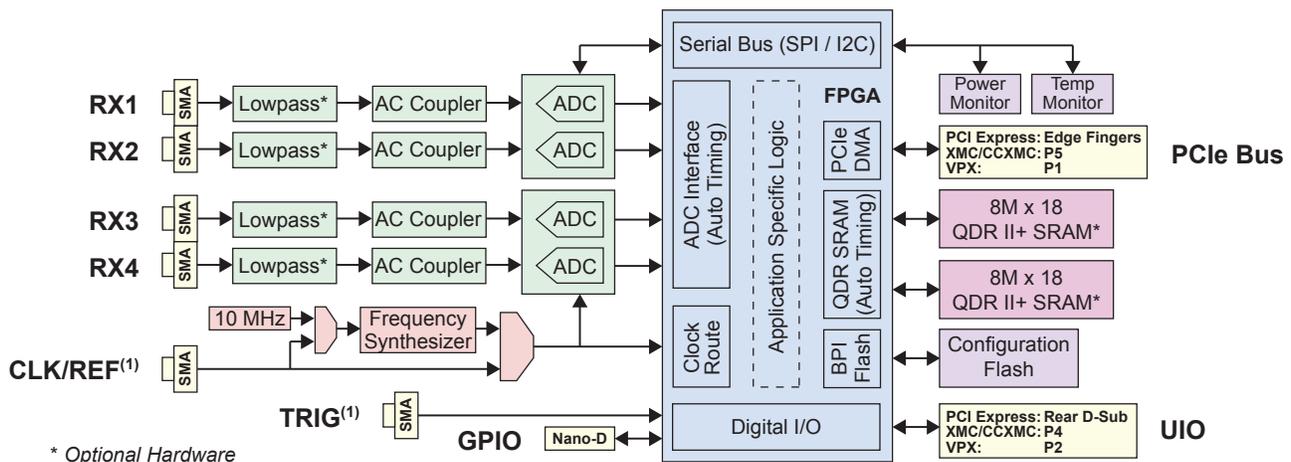
The Model 377 is designed around the Texas Instruments ADS42LB69 16-bit dual ADC. The 250 MHz sample clock is supplied by either the on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz TCXO or an external reference can be used to achieve system-wide phase coherence.

Adopting open architecture hardware and software standards allows SigFPGA™ products to seamlessly transition from the desktop to embedded platforms.

### Typical Applications

| | |
|---|---|
| Spectrum monitor | Test & measurement |
| Radar & comms | Acqusition & telemetry |
| Signal recorder | Medical diagnostics |
| Software defined radio | DSP accelerator |

**Four AC coupled 16-bit ADC channels**

**Three Xilinx Kintex-7 FPGA size options**

**Two banks of optional QDR II+ SRAM**

**Internal or external sample clock (≤ 250 MHz)**

**Phase locked frequency synthesizer**

**Internal or external 10 MHz reference**

**Temperature and power supply monitors**

**PCI Express (PCIe) x8 or x4 host bus**

**High performance scatter-gather DMA**

**Front and rear auxiliary connectors**

**Configuration flash loads from JTAG or host**

**FPGA VHDL core library for data interfaces**

**FPGA VHDL reference design with source**

**Demostation software (C) with source**

## Form Factor

| | |
|---|---|
| PCI Express (air cooled) | PCI Express 2.1, standard height, half-length, x8 or x4 physical edge connector |
| XMC (air cooled) | ANSI/VITA 42.0 single-width, ANSI/VITA 42.3 |
| CCXMC (conduction cooled) | XMC plus ANSI/VITA 20 |
| VPX (air or conduction cooled) | 3U Eurocard, VITA 65, front panel I/O |

## FPGA Selection

| | |
|---|---|
| Device | Xilinx Kintex-7 |
| Size | XC7K160T, XC7K325T, or XC7K410T |
| Speed/Temperature Grade | -2I (Industrial) or -3E (Extended) |

## Optional SRAM

| | |
|---|---|
| Technology | QDR II+ 8M x 18 b4 |
| Performance | 1.8 GB/s simultaneous r/w per bank |
| Capacity | 32 MB across two banks of 16 MB |

## Digital I/O

| | |
|---|---|
| PCI Express Bus on Edge Fingers (PCI Express), P5 (XMC/CCXMC), P1 (VPX) | x8 or x4 electrical, Gen 2 backward compatible with Gen 1 and upward comaptible with Gen 3 |
| General Purpose I/O (GPIO) on 15-pin Nano-D | 6-bit LVTTL (3.3V), plus single 50 Ω or Hi-Z terminated LVTTL (3.3V / 5V tolerant) trigger |
| User I/O (UIO) on 68-pin D-Sub (PCI Express), P4 (XMC/CCXMC), P2 (VPX) | 48-bit LVTTL (3.3V or 2.5V) or 24-bit LVDS, plus 12-bit LVTTL (3.3V or 2.5V), plus 2-bit LVTTL (voltage determined by 48-bit selection) |
| Trigger [1] (TRIG) on SMA | 50 Ω, (3.3V / 5V tolerant) LVTTL |

## Analog I/O

| | |
|---|---|
| Receiver (RX) on SMA | 50 Ω, ADC input |
| Clock/Reference [1] (CLK/REF) on SMA | 50 Ω, external sample clock or 10 MHz reference to internal sample clock |

## Power [4] (No SRAM / 32MB SRAM)

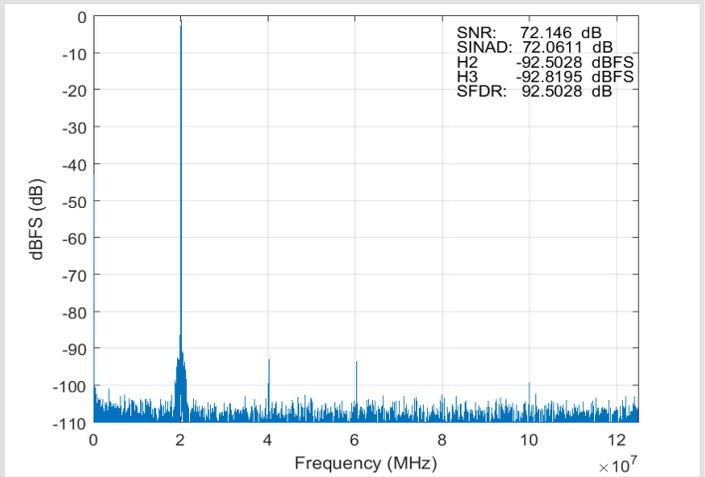| | |
|---|---|
| PCI Express [5] | 12V = 10.0W / 15.7W, 3.3V = 27mW |
| XMC or CCXMC [5] | 12V = 2.3W, VPWR = 3.2W / 9.0W, 3.3V = 2.8W |
| VPX [5] | 12V = 5.5W / 11.2W, 3.3V = 2.8W |

## Environmental [6]

| | |
|---|---|
| Storage Temperature | -55 ºC to 125 ºC |
| Operating Ambient Temperature | -30 ºC to 85 ºC |
| Typical Air Flow [7] | 150 LFM |
| Max Heat Sink Temperature | 95 ºC |

## Software

| | |
|---|---|
| Driver (32-bit or 64-bit) | Windows 7/8/10, Linux |
| API & Demonstration Code | C (C++ compatible) |

## Typical Performance Characteristics [2]



```
SNR:    72.146  dB
SINAD:  72.0611 dB
H2      -92.5028 dBFS
H3      -92.8195 dBFS
SFDR:   92.5028 dB
```

## Receiver (RX) Performance

| | |
|---|---|
| Passband | 1 to 250 MHz (1 dB), 0.1 to 500 MHz (3 dB) |
| Full Scale Input Amplitude | 10.8 dBm [2] (2.2 Vpp [2]), 12.8 dBm [3] (2.8 Vpp [3]) |
| SNR (20.17 MHz Input) | 73.5 dB [2], 74.8 dB [3] |
| SINAD (20.17 MHz Input) | 73.4 dB [2], 74.7 dB [3] |
| SFDR (20.17 MHz Input) | 90 dBc [2], 87 dBc [3] |
| Channel Isolation (50 MHz) | 90 dB |
| Optional Lowpass Filter | 5-pole Butterworth or Chebychev |

## Clock/Reference (CLK/REF) Performance

| | |
|---|---|
| Clock Frequency (Fs) Range | 50 to 250 MHz |
| Internal Clock Phase Noise | -100 dBc/Hz (10 kHz offset) |
| Internal Reference Accuracy | 10 MHz +/- 1 ppm |
| External Clock Amplitude | 2 dBm (0.8 Vpp) to 13 dBm (2.8 Vpp) |
| External Reference Amplitude | 7 dBm (1.5 Vpp) to 14.8 dBm (3.5 Vpp) |

## Single Piece Price [8]

| | |
|---|---|
| XC7K160T-2I | $4,740 (No SRAM) / $5,740 (32 MB SRAM) |
| XC7K325T-2I | $5,500 (No SRAM) / $6,500 (32 MB SRAM) |
| XC7K410T-2I | $6,260 (No SRAM) / $7,260 (32 MB SRAM) |
| XC7K160T-3E | $5,000 (No SRAM) / $6,000 (32 MB SRAM) |
| XC7K325T-3E | $6,000 (No SRAM) / $7,000 (32 MB SRAM) |
| XC7K410T-3E | $7,000 (No SRAM) / $8,000 (32 MB SRAM) |

## Contact Information

| | |
|---|---|
| Address | Red Rapids<br>797 N Grove Rd, Suite 101<br>Richardson, TX  75081 |
| Phone | 972-671-9570  (+1 country code) |
| Website | www.redrapids.com |
| E-mail | sales@redrapids.com |

[1] Both the TRIG and CLK/REF inputs are available on the PCI Express form factor, all other form factors are limited to either one as a build option.
[2] Measurement with ADC programmed to default 2.0 Vpp full-scale input voltage range.
[3] Measurement with ADC programmed to maximum 2.5 Vpp full-scale input voltage range.
[4] Voltage monitors attached to the primary supply inputs provide measurements accessible through the software API.
[5] Voltages that do not supply power are omitted. Values do not include power consumed by the application specific FPGA logic. FPGA power is drawn from the VPWR source on XMC/CCXMC units and 12V on all others. FPGA logic power will incur a 10% efficiency loss through voltage converters.
[6] Temperature monitors distributed across the board provide measurements accessible through the software API.
[7] Required air flow will depend on the power consumed by the FPGA which is application specific.
[8] Prices shown for PCI Express, XMC, and CCXMC form factors; add $2,000 for the VPX form factor.