Front End 000-010
Single 12-Bit 1500 Msps Receiver
Reference Manual

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1.0 Introduction

1.1 Contents and Structure

This manual describes the Front End 000-010 receiver hardware. The focus of this manual is the electrical function of the hardware including control structure, signal flow and key components.

The latest product documentation and software is available for download from the Red Rapids web site (www.redrapids.com).

1.2 Conventions

This manual uses the following conventions:

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are acronyms used in this manual.

- **AC** Alternating Current (Greater than 0 Hertz)
- **ADC** Analog to Digital Converter
- **DAC** Digital to Analog Converter
- **dB** Decibels
- **dBFS** Decibels Relative to Full Scale
- **dBm** Decibels Relative to One milliwatt
- **DC** Direct Current (0 Hertz)
- **DDR** Double Data Rate
- **FFT** Fast Fourier Transform
- **LVDS** Low Voltage Differential Signaling
- **MHz** Megahertz
- **mV** millivolts
- **Msps** Mega Samples per Second
- **PGA** Programmable Gain Amplifier
- **RF** Radio Frequency
- **SFDR** Spur Free Dynamic Range
- **SINAD** Signal-to-Noise and Distortion Ratio
- **SNR** Signal-to-Noise Ratio
- **SPI** Serial Peripheral Interface
- **Vpp** Voltage, peak-to-peak

1.3 Revision History

Version	Date	Description
R00	04/05/2016	Initial release.

2.0 Description

The Front End 000-010 receiver is a high performance single-channel structure built around the Texas Instruments ADC12D1000 12-Bit 1.0/2.0 GSPS Ultra-High-Speed ADC.

Features[1]:

- Single Channel
- 12-bit Architecture
- SNR 58.5 dB
- SFDR 60 dB
- DES Sample Rate up to 1500 Msps
- 1300 MHz Full Power Bandwidth (AC-Coupled)
- 1100 MHz Full Power Bandwidth (DC-Coupled)
- AC or DC Coupled (build option)
- Precision DC offset adjustment (DC-Coupled option)

Note [1]: Features listed are mode and build dependent. See specifications and performance sections for more information.

A block diagram of the receiver section is shown in Figure 2-1. The receiver section consists of a single analog receiver channel labeled RX 1. A receiver channel consists of a front panel SMA connector, a coupling mechanism and an ADC. The analog input is digitized by the ADC and the ensuing data samples are streamed to the Data Interface. Data timing is controlled via a high-speed precision sample clock distributed through a low noise network. ADC features are programmed through the Control Interface. The following paragraphs provide details about each element of the receiver section.

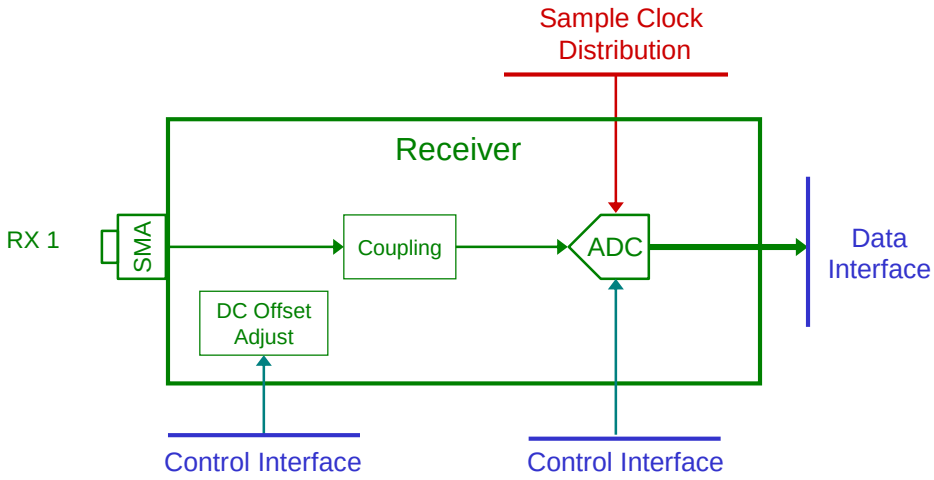


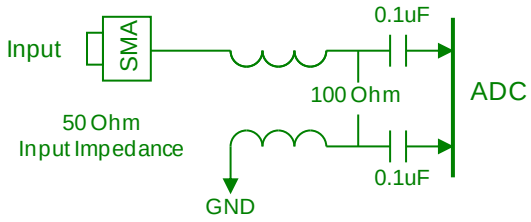
Figure 2-1 Receiver Block Diagram

2.1 Coupling

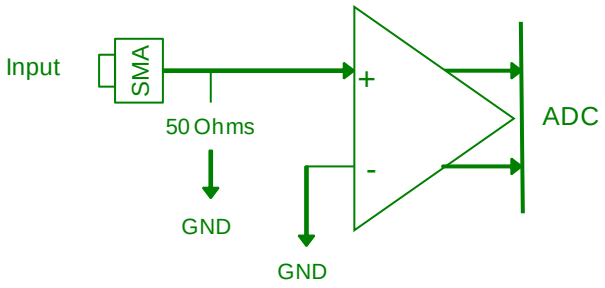
The receiver is available AC or DC coupled as a build option as shown in Figure 2-2. AC coupled units typically offer better high frequency performance and SNR at the expense of low frequency operation. DC-coupled units provide for good low frequency operation down to DC at the expense of added noise and distortion from the coupling amplifier.

AC units block DC signal content with a 0.1 uF series capacitor and are transformer coupled to the ADC. DC-coupled units use a differential amplifier to couple the input signal to the ADC. DC-coupled units require a dc-coupled system source impedance of 50 Ohms to ensure proper coupling amplifier bias. Other source impedances are supported as a build option.

> ☞ DC-coupled units require a dc-coupled source impedance of 50 Ohms as part of double balanced system.



AC-Coupled Build Option



DC-Coupled Build Option

Figure 2-2 Coupling Options (equivalent circuits)

2.2 DC Offset Adjustment (DC-Coupled option only)

The DC-coupled receiver option contains a set of DACs to trim larger DC offset errors that are induced by the coupling amplifier and system DC mismatch. A block diagram of the trim DAC structure is shown in Figure 2-3 for a single analog input. The DC offset trimming function is implemented using a dual DAC in a push-pull configuration. DAC A offsets the ADC input voltage in a positive direction while DAC B offsets the ADC input in a negative direction. Trim DAC register settings can be found in the device data sheet listed in section 5.0. The receiver trim DACs are accessed through the Control Interface via a SPI bus as shown in Figure 2-4.

> ☞ Only one of the pair of offset trim DACs per input should be active at a time. The unused trim DAC should be set to 0 V.

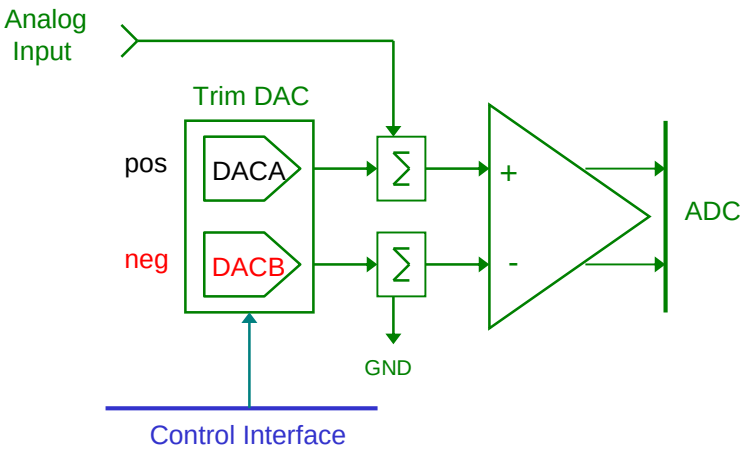


Figure 2-3 Trim DAC Operation in DC-Coupled Build Option

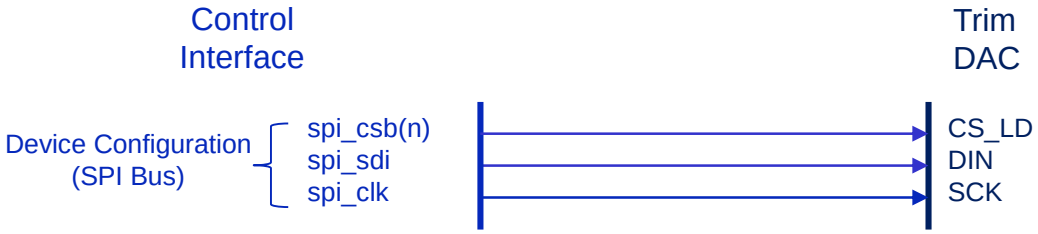


Figure 2-4 Trim DAC Control

2.3 ADC Configuration

The receiver ADC has a number of configuration options available to support different modes of operation. These operational modes are described in the ADC device data sheet listed in section 5.0. The following paragraphs describe how the ADC is configured for use in Front End 000-010.

2.3.1 ADC Hardware Configuration

A summary of the ADC device hardware configuration is provided in Table 2-1. A diagram of the ADC input configuration is shown in Figure 2-5. This table describes ADC device control pin physical connections. Pin names are taken from the device data sheet listed in section 5.0.

Table 2-1 Receiver ADC Hardware Configuration

Device Pin Name	Connection	Description
ECE_N	Pull down	1.0k Ohm to ground (Extended control enabled)
VCMO	Pull down (AC Coupled) Float (DC Coupled)	0 Ohm to ground (AC coupled mode). Used as VCOM (DC coupled mode)
VBG	Pull up	0 Ohm to Va (supply), 1.2 V LVDS.
REXTP/N	Precision resistor	Precision 3.3k Ohm resistor between terminals
RXTRIMP/N	Precision resistor	Precision 3.3k Ohm resistor between terminals
DCLK_RSTP DCLK_RSTN	Pull down Pull up	1.0k Ohm to ground. 1.0k Ohm to Va (supply)
RCLKP/RCLKN	NC	Not connected
RCOUT1P/N	NC	Not connected

RCOUT2P/N	NC	Not connected
PDI, PDQ, TPM, DDRH	Pull down	1.0k Ohm to ground.
CLK_P/N	Sample Clock	Connected to sample clock distribution network
VINIP/VININ	RX Input 1	RX channel 1 input
VINQP/VINQN	Terminated into 50 Ohms	Not used, terminated for DESI mode.
DES	Pull down	1.0k Ohm to ground.
CAL	Pull down	1.0k Ohm to ground.
CalDly	Pull up	1.0k Ohm to Va (supply)
CalRun	Pull down	1.0k Ohm to ground.
NDM	Pull up	1.0k Ohm to Va (supply), Non De-Mux Mode.
FSR	Pull up	1.0k Ohm to Va (supply)

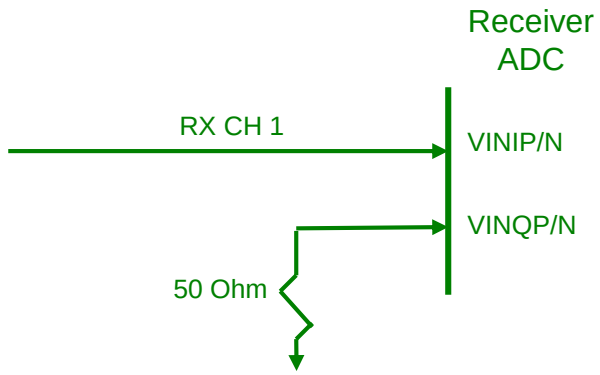


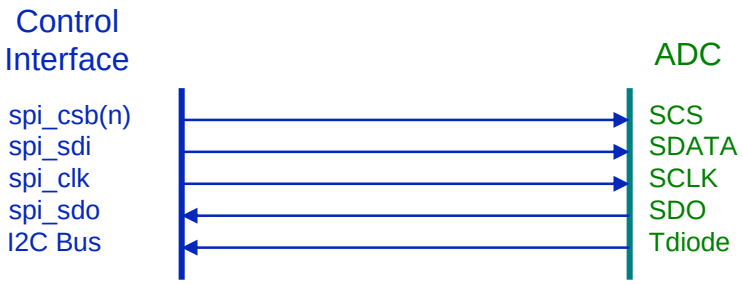
Figure 2-5 ADC Input Configuration

2.3.2 ADC Control Interface

Table 2-2 provides a list of ADC Control Interface connections. A diagram of ADC Control Interface is shown in Figure 2-6. The user has access to the ADC command and status registers through the Control Interface SPI port. A list and description of ADC command and status registers can be found in the device data sheet listed in section 5.0.

Table 2-2 ADC Control Interface Connections

Device Pin Name	Control Interface Name	Description
SCSN	spi_csb(n)	SPI port chip select
SDATA	spi_sdi	SPI port data in
SCLK	spi_clk	SPI port clock
SDO	Spi_sdo	SPI port data out
TdiodeP/N	temp monitor (I2C bus)	ADC die temperature



(n) = User Interface bit assignment

Figure 2-6 ADC User Control Interface

2.3.3 ADC Clock Interface

The receiver ADC clock input is sourced by the sample clock distribution network as shown in Figure 2-7. The ADC input clock rate is half the DES sample rate when the device is commanded to Non De-Mux, DES mode.

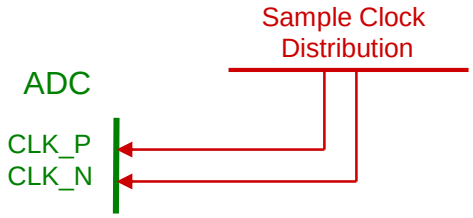


Figure 2-7 ADC Clock Interface

2.3.4 ADC Data Interface

A diagram of the ADC Data Interface is shown in Figure 2 5. The RX1 input is digitized and output through the I and Q data outputs at half the DES sample rate when the device is commanded to Non De-Mux, DES mode. The ADC outputs a forwarded data clock that runs at the reduced rate. Please see the ADC datasheet referenced in section 5.0 for more information on data transfer.

Table 2-3 ADC Data Interface Connections

Device Pin Name	Data Interface Name	Description
ORI_P/N	RX1_OVR_P/N	RX1 over range bit
ORQ_P/N	RX2_OVR_P/N	RX1 delayed over range bit (DES Mode)
DI(11:0)P/N	RX1P/N(11:0)	RX1 data (DES Mode)
DId(11:0)P/N	DRX1P/N(11:0)	Not used (DES Mode)
DQ(11:0)P/N	RX2P/N(11:0)	RX1 delayed data (DES Mode)
DQd(11:0)P/N	DRX2P/N(11:0)	Not used (DES Mode)
DCLKI_P/N	SAMPLE_CLK_P/N	RX1 data clock (DES Mode)
DCLKQ_P/N	DCLKQP/N	RX1 delayed data clock (DES Mode)

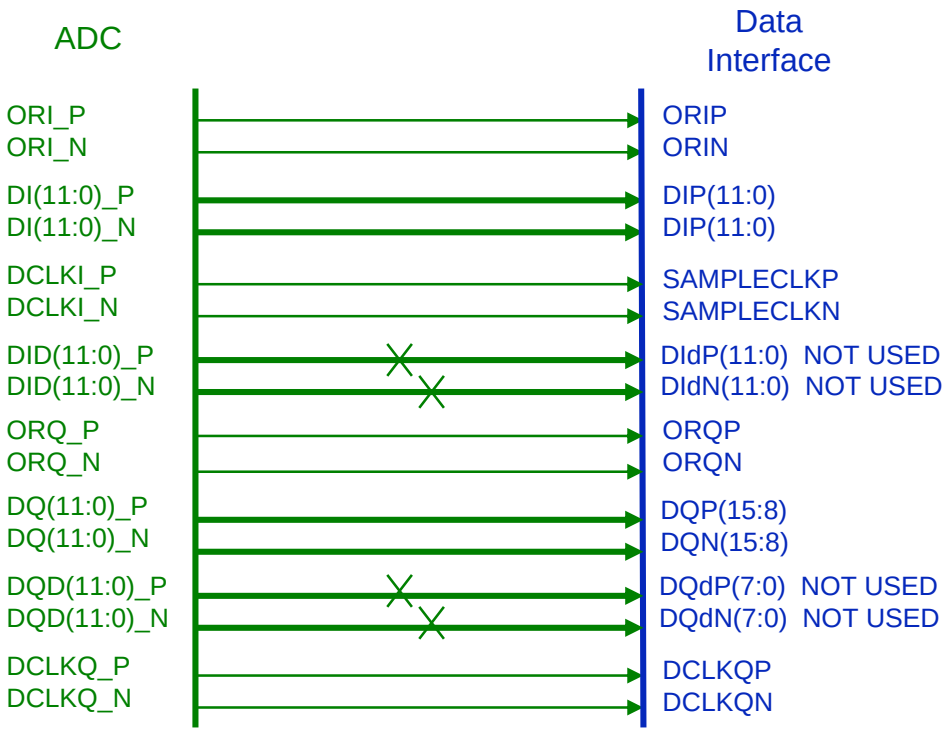


Figure 2-8 ADC User Data Interface

3.0 Specifications

The following section lists the performance specifications of the Front End Receiver based on direct unit measurement unless otherwise noted. Measurements are listed as typical and represent the mean performance of a representative sample of units under laboratory conditions as listed in Table 3-1. More information on test setup can be found in section 4.1. Some variation in performance will occur based on build variation, external system performance and environment. See key component device data sheets in section 5.0 for more insight on performance variation.

Table 3-1 Test Environment

Item	Description
Host	Personal Computer, On carrier in PCIe x8 Slot
Air Temperature	25 C (Room)
Cooling	Convection (Fan)
Voltage	Nominal “Typical” levels
Clock	750 MHz External Clock (except where noted)

3.1 Input Levels

Parameter	Min	Typ	Max	Unit
Input Impedance		50		Ohms
Full Scale Input (0 dBFS, FSR = 800mV))				
AC-Coupled Mode (Power into 50 Ohms)				
100 MHz		+2.7		dBm
500 MHz		+3.3		dBm
1000 MHz		+4.5		dBm
1500 MHz		+7.4		dBm
2000 MHz		+10.7		dBm
DC-Coupled Mode (Power into 50 Ohms)				
100 MHz		+4		dBm
200 MHz		+4.1		dBm
300 MHz		+4.3		dBm
400 MHz		+3.4		dBm
500 MHz		+2.1		dBm

Performance

> ☞ Performance may vary depending on the quality of the power supply and EMI environment of the host.

3.1.1 AC-Coupled

Measurement conditions: T = 25°C, Supply Voltages (+12, 3.3) nominal

Parameter	Min	Typ	Max	Unit
Performance				
Passband[1]				
1 dB bandwidth	10		600	MHz
3 dB bandwidth	0.1		1300	MHz
6 dB bandwidth	0.05		1800	MHz
SNR[2]				
124.8 MHz				
500 (1000)		57.4		dB
666 (1333)		57.1		dB
750 (1500)		56.0		dB
248.7 MHz				
500 (1000)		57.3		dB
666 (1333)		57.7		dB
750 (1500)		55.6		dB
SINAD[2]				
124.8 MHz				
500 (1000)		56.4		dB
666 (1333)		56.3		dB
750 (1500)		54.7		dB
248.7 MHz				
500 (1000)		56.3		dB
666 (1333)		55.7		dB
750 (1500)		54.2		dB
SFDR[2]				
124.8 MHz				
500 (1000)		67.1		dB
666 (1333)		67.1		dB
750 (1500)		62.5		dB
248.7 MHz				
500 (1000)		64.9		dB
666 (1333)		63.5		dB
750 (1500)		61.6		dB
Channel Isolation[3] (MHz)				
100		69		dB
500		58		dB
1000		54		dB
1500		49		dB
2000		44		dB
2500		44		dB

Notes:
[1]Measured across band using ADC output.
[2]Measured at indicated frequency using an 8192 point FFT for three clock rates listed, 500 (1000 DES) MHz/750 (1500 DES) MHz External and 666 (1333 DES) MHz Internal.
[3]Measured on terminated channel with -1 dBFS input signal in adjoining channel.

3.1.2 DC-Coupled

Measurement conditions: T = 25°C, Supply Voltages (+12, 3.3) nominal

Parameter	Min	Typ	Max	Unit
Performance				
Passband[1]				
1 dB bandwidth	DC		1000	MHz
3 dB bandwidth	DC		1100	MHz
6 dB bandwidth	DC		1300	MHz
SNR[2]				
124.8 MHz				
500 (1000)		53.5		dB
666 (1333)		53.4		dB
750 (1500)		52.6		dB
248.7 MHz				
500 (1000)		54.8		dB
666 (1333)		52.0		dB
750 (1500)		51.7		dB
SINAD[2]				
124.8 MHz				
500 (1000)		53.3		dB
666 (1333)		53.2		dB
750 (1500)		52.4		dB
248.7 MHz				
500 (1000)		51.3		dB
666 (1333)		49.7		dB
750 (1500)		49.7		dB
SFDR[2]				
124.8 MHz				
500 (1000)		69		dB
666 (1333)		69		dB
750 (1500)		66		dB
248.7 MHz				
500 (1000)		58		dB
666 (1333)		56		dB
750 (1500)		57		dB
Channel Isolation[3] (MHz)				
1		79		dB
100		61		dB
200		55		dB
300		51		dB
400		49		dB
500		47		dB

Notes:

[1]Measured across band using ADC output.

[2]Measured at indicated frequency using an 8192 point FFT for three clock rates listed, 500 (1000 DES) MHz/750 (1500 DES) MHz External and 666 (1333 DES) MHz Internal.

[3]Measured on terminated channel with -1 dBFS input signal in adjoining channel.

3.2 Absolute Maximums

Stresses above those listed in Table 3-2 may cause damage to the unit. The operation of the unit at these or any other conditions outside of those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

Table 3-2 Absolute Maximum Specifications

Parameter	Min	Typ	Max	Unit
Receiver Inputs (50 Ohms)				
AC-Coupled				
DC Input Voltage	-10		10	V
AC Voltage Swing			3.6	Vpp
AC Input Power			+15	dBm
DC-Coupled				
Absolute DC Input Voltage	-2.5		+2.5	V
AC Voltage Swing			3.6	Vpp
AC Input Power			+15	dBm

! Exposure to absolute maximum conditions for extended periods may degrade unit reliability.

4.0 Typical Performance Characteristics

The following sections contain spectrum plots of the receiver showing typical performance for a variety of sine wave inputs. Each sine input is characterized using an 8k point FFT.

4.1 AC-Coupled

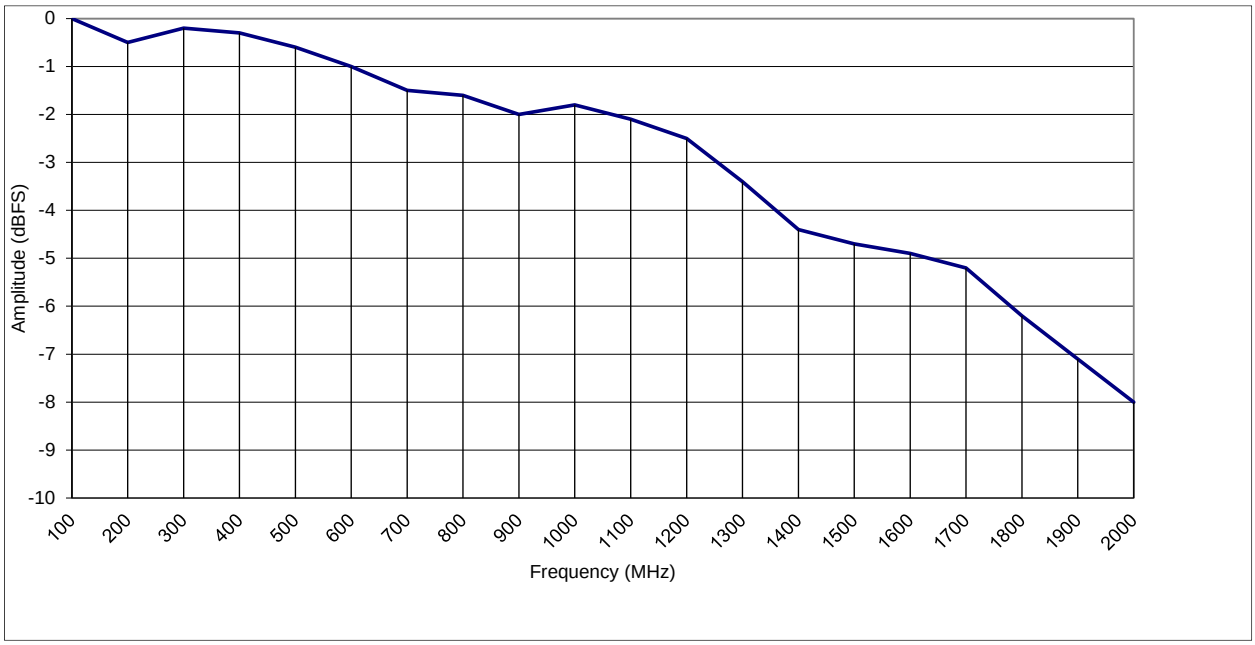


Figure 4-1 Passband Profile 100 to 2000 MHz

4.1.1 500 (1000 DES rate) MHz External Sample Clock

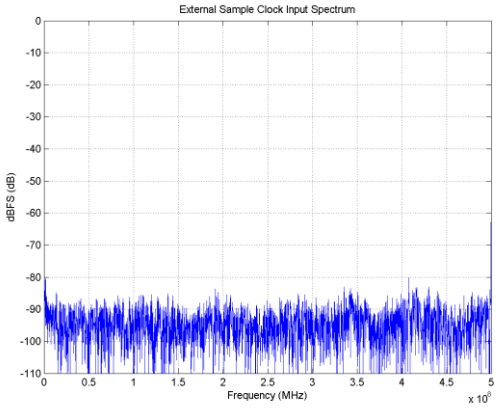


Figure 4-2 Terminated Input

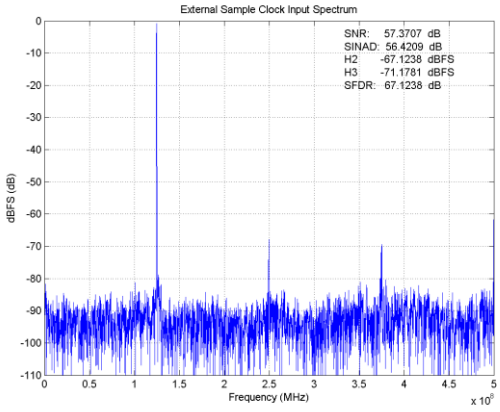


Figure 4-3 124.8 MHz Input, -0.5 dBFS

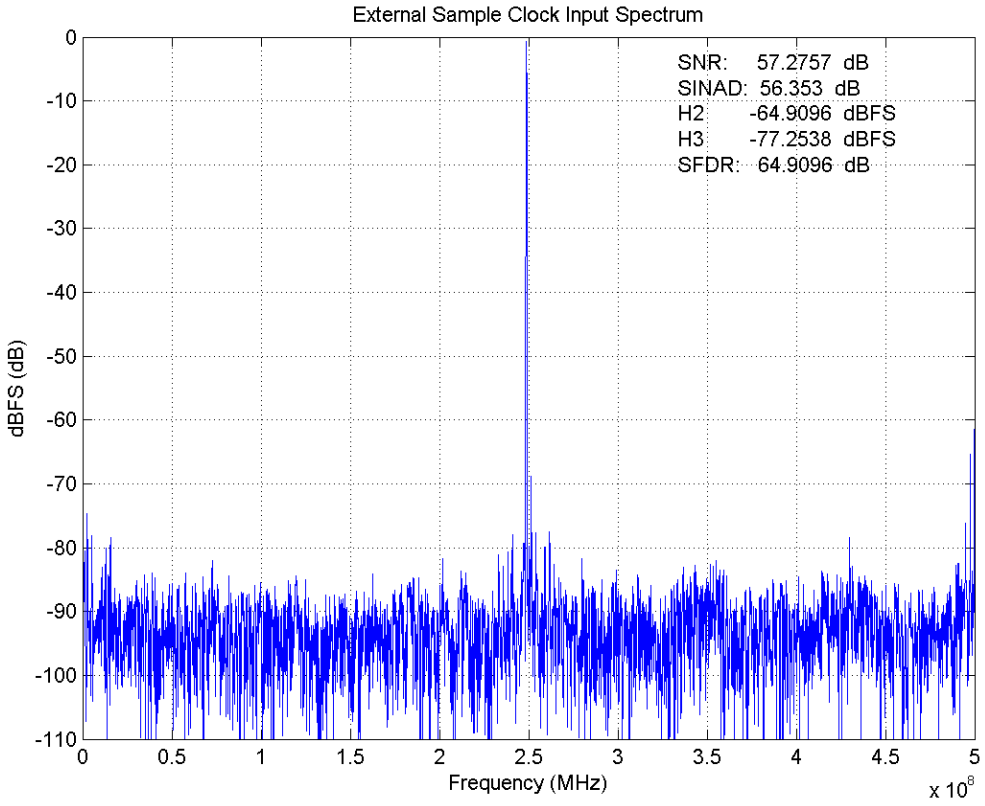


Figure 4-4 248.7 MHz Input, -0.5 dBFS

4.1.2 666 (1333 DES rate) MHz Internal Synthesizer

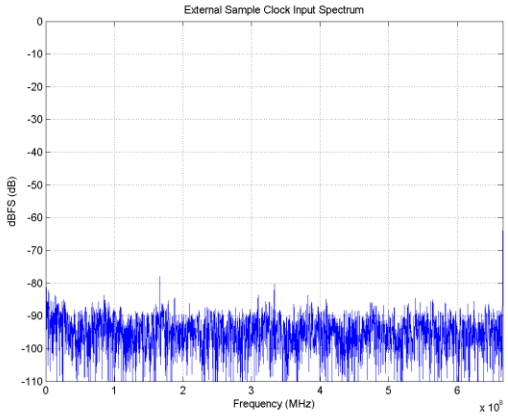


Figure 4-5 Terminated Input

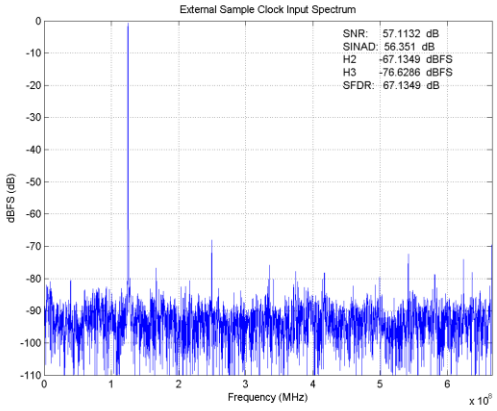


Figure 4-6 124.8 MHz Input, -0.5 dBFS

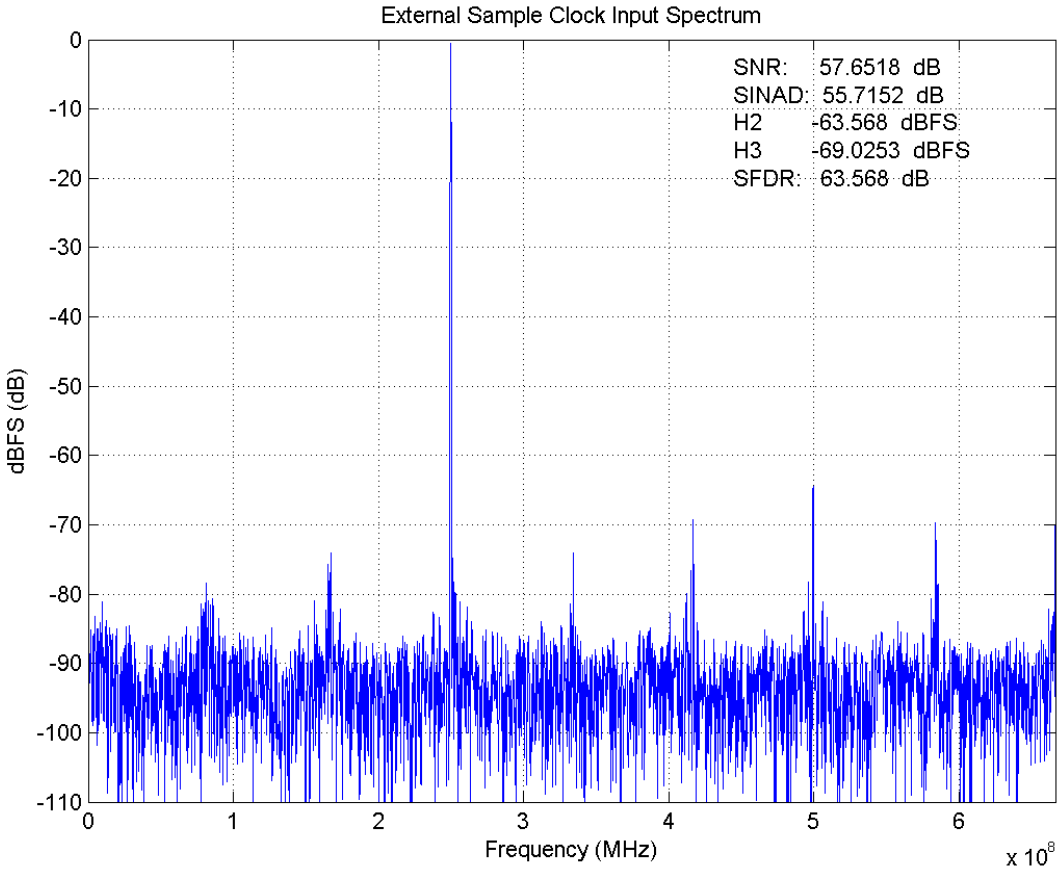


Figure 4-7 248.7 MHz Input, -0.5 dBFS

4.1.1 750 (1500 DES rate) MHz External Clock

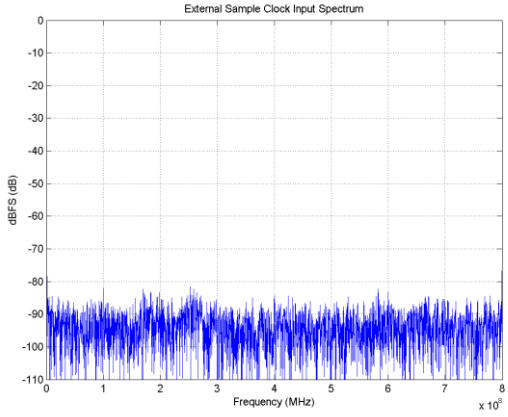


Figure 4-8 Terminated Input

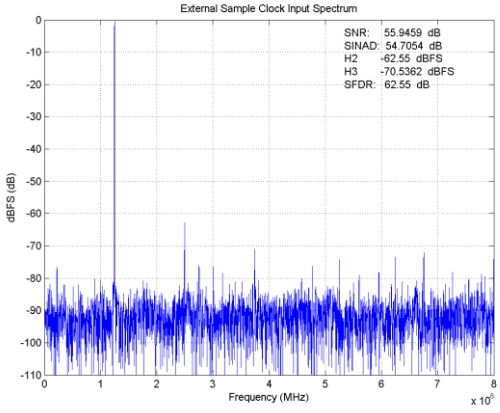


Figure 4-9 124.8 MHz Input, -0.5 dBFS

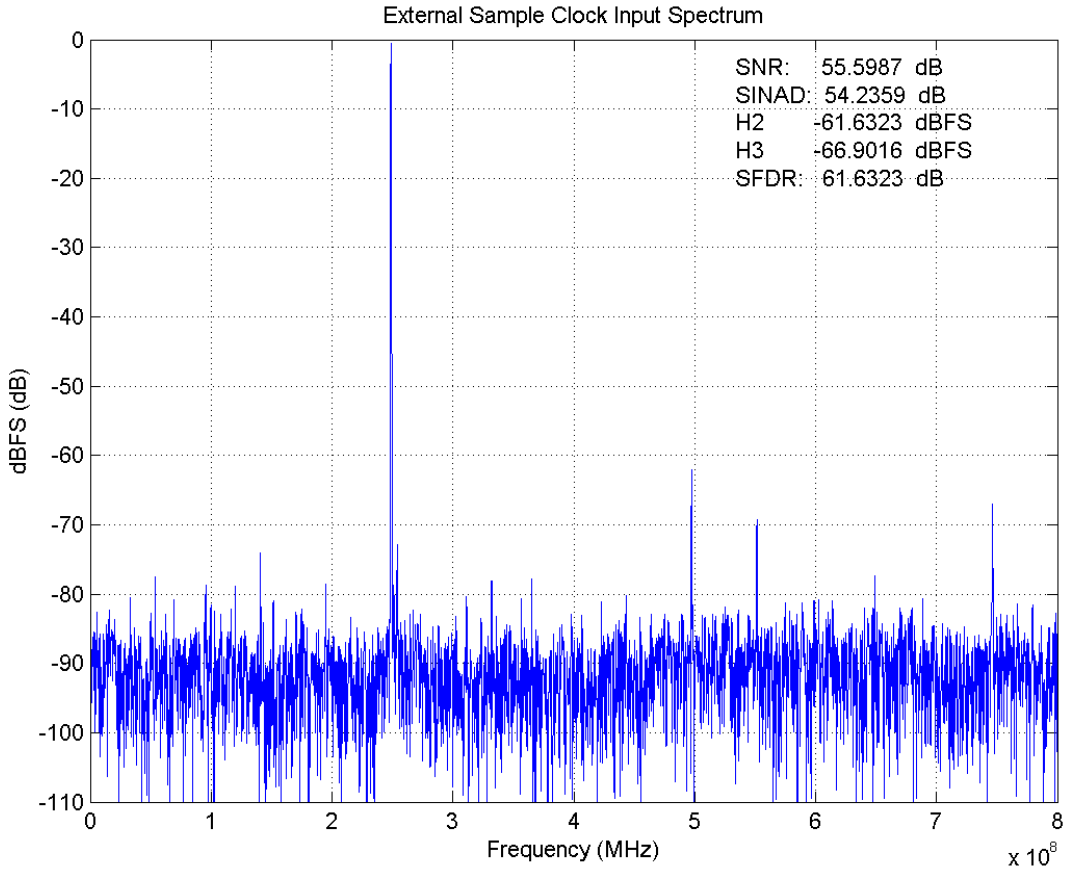


Figure 4-10 248.7 MHz Input, -0.5 dBFS

4.2 DC-Coupled

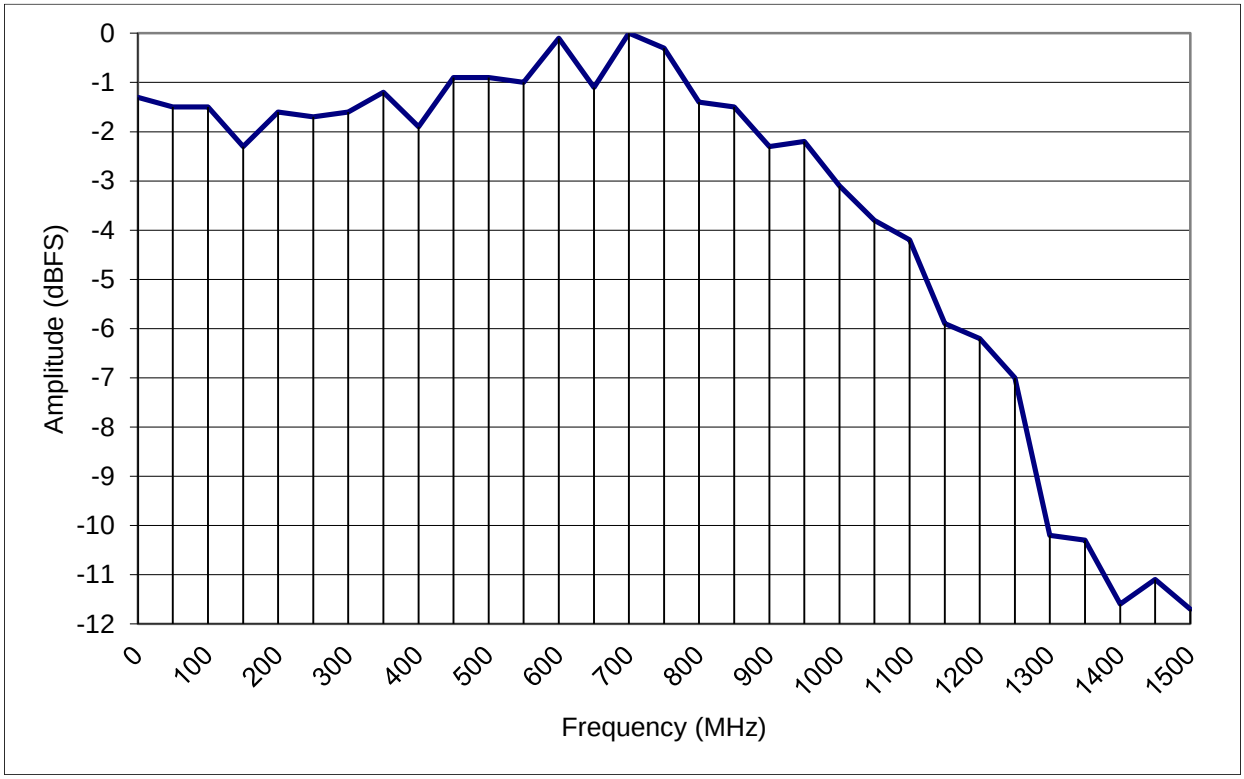


Figure 4-11 Passband Profile DC to 1500 MHz

4.2.1 500 (1000 DES rate) MHz External Sample Clock

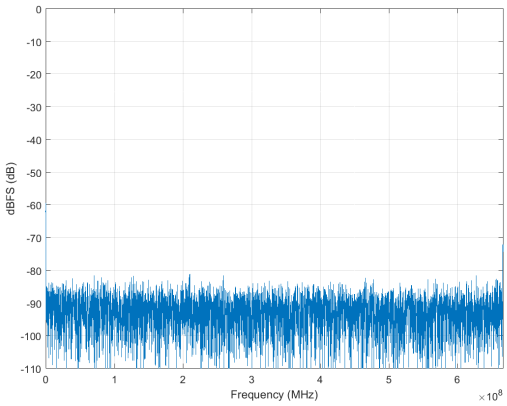


Figure 4-12 Terminated Input

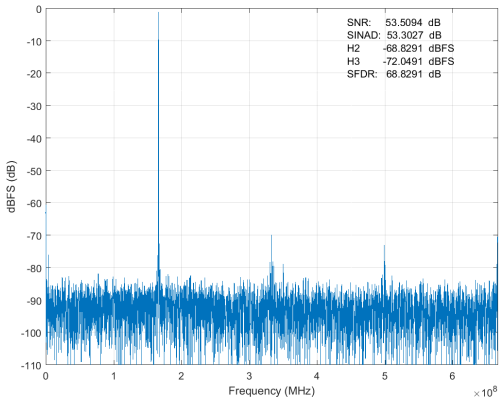


Figure 4-13 124.8 MHz Input, -1.0 dBFS

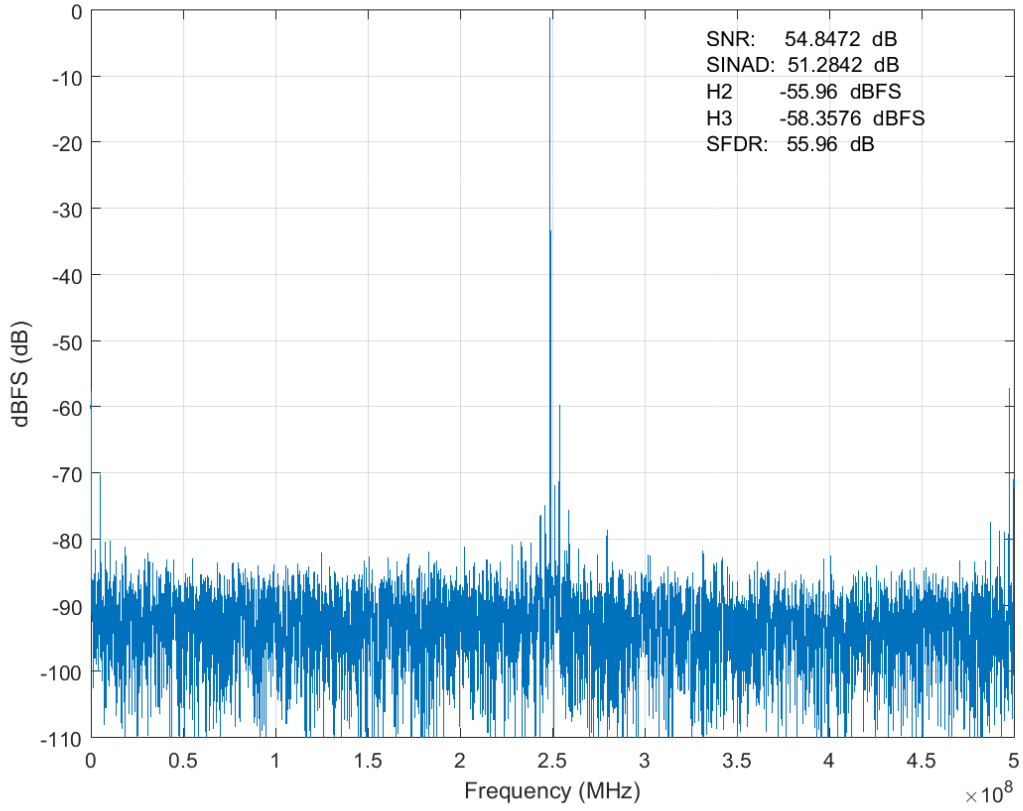


Figure 4-14 248.7 MHz Input, -1,0 dBFS

4.2.2 666 (1333 DES rate) MHz Internal Synthesizer

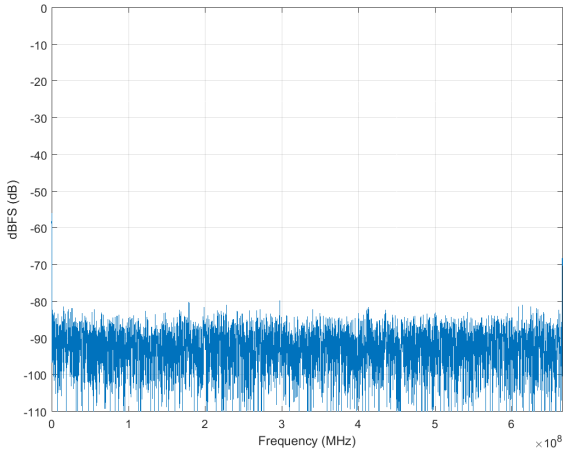


Figure 4-15 Terminated Input

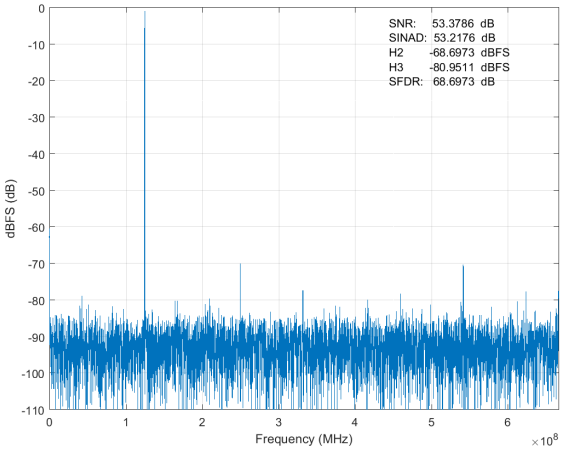


Figure 4-16 124.8 MHz Input, -1.0 dBFS

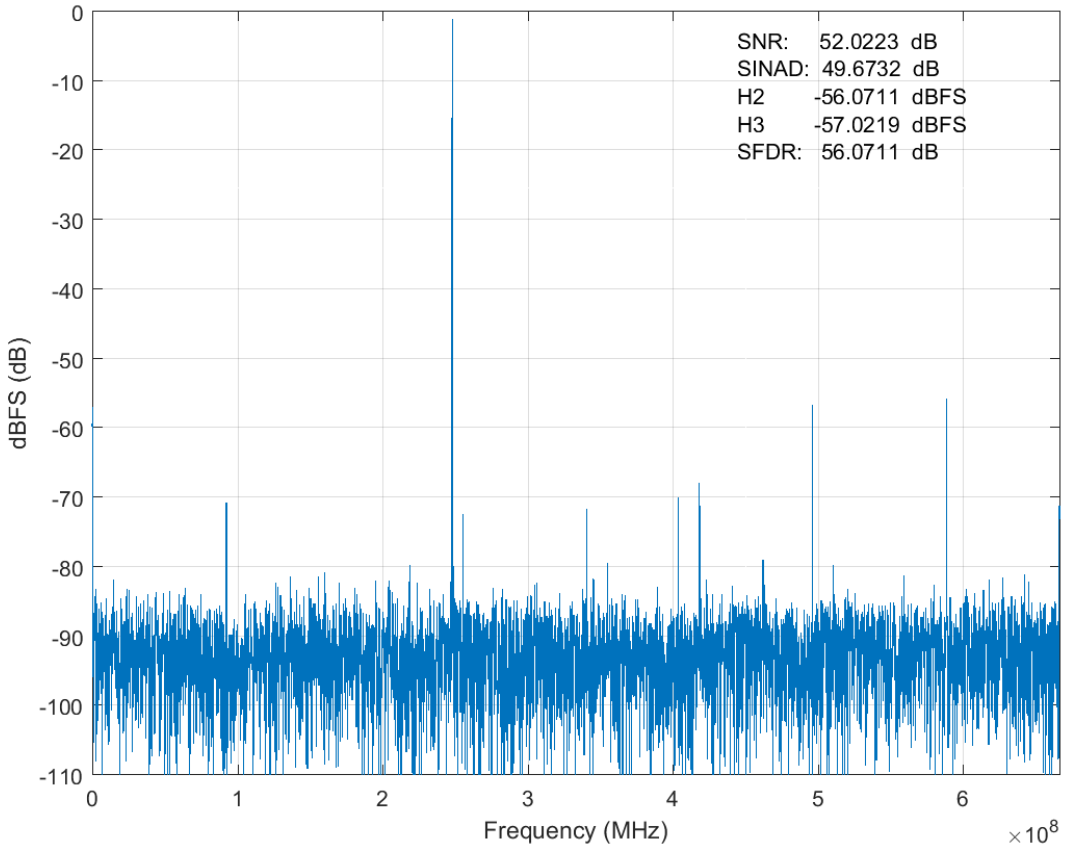


Figure 4-17 248.7 MHz Input, -1.0 dBFS

4.2.3 750 (1500 DES rate) MHz External Clock

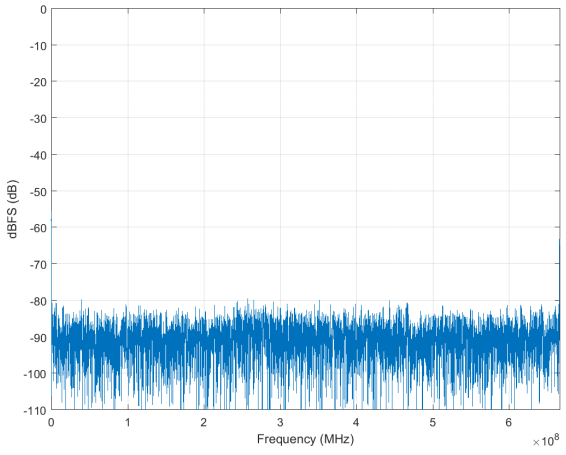


Figure 4-18 Terminated Input

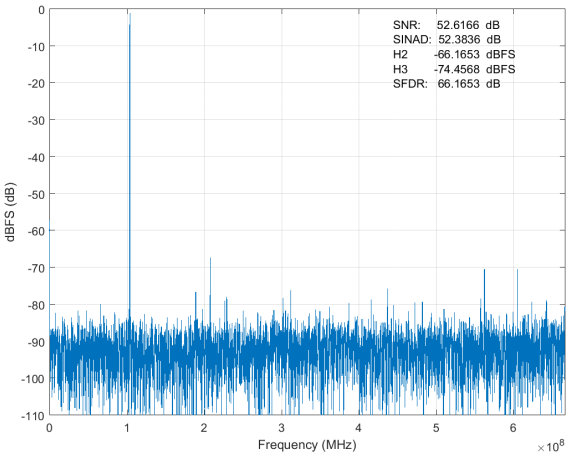


Figure 4-19 124.8 MHz Input, -1.0 dBFS

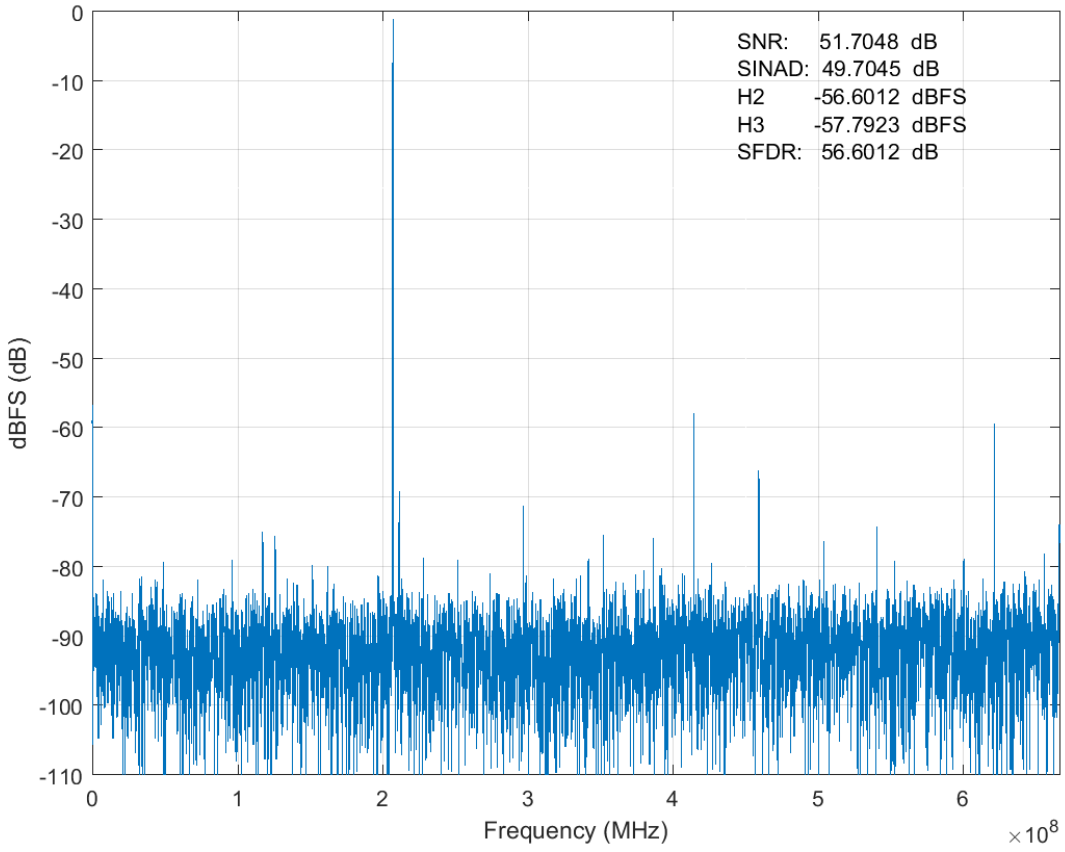


Figure 4-20 248.7 MHz Input, -1.0 dBFS

4.3 Generating Characterization Plots

The wide dynamic range and input bandwidth characteristics of the receiver levy strict signal conditioning requirements on test equipment used to characterize board performance. Even the highest quality general purpose RF signal generators output harmonics and noise that must be reduced in order to accurately characterize system performance. Generally a narrow bandpass filter is inserted between the signal generator output and the receiver front end. The bandpass filter should be reasonably narrow to eliminate generator harmonics and limit the amount of generator phase noise input into the receiver. Red Rapids' characterization plots were created using 5% bandwidth 7-section Chebyshev filters with > 55 dB of stop band rejection. We used filters from TTE such as their KC7t-70m-3.5m-50-720a. Table 4-1 contains a list of test equipment used to generate the characterization plots of section 4.0. The characterization frequency plots were generated by performing an 8k FFT on 8k data samples collected from the receiver.

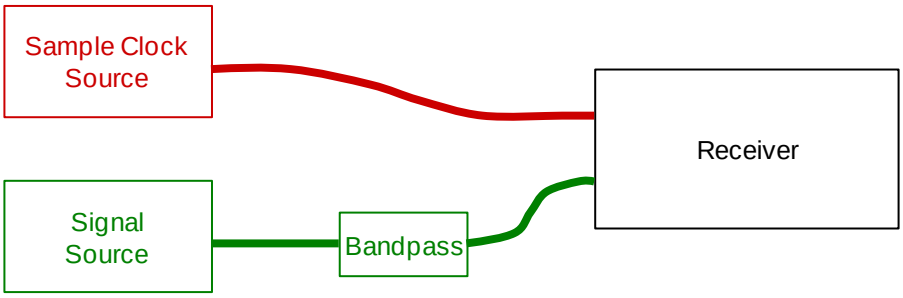


Figure 4-21 Characterization Setup

☞ Use a narrow bandpass filter between the signal generator and receiver card to accurately characterize system.

Table 4-1 Characterization Test Equipment

Function	Part Number	Manufacturer
Sample Clock Source	HP8648B	Agilent
Signal Bandpass Filter (one of several)	KC7t-70m-3.5m-50-720a	TTE
Signal Source	HP8648B	Agilent

5.0 Key Components

Key hardware components for the Receiver are listed in Table 5-1. Device datasheets can be downloaded from vendor websites for more information.

Table 5-1 Key Hardware Components

Component	Part Number	Vendor	Comments
Receiver ADC	ADC12D1000CIUT/NOPB	Texas Instruments	12-Bit 1.0/2.0 GSPS Ultra High-Speed ADC
Trim DAC	LTC1661CMS8#PBF	Linear Technology	Dual 10-bit Micropower DAC

6.0 Technical Support

Please feel free to contact us if you have a technical question about or problem with our product. We understand that our customers have tight deadlines and time is of the essence in development and production cycles. We will make every effort to resolve problems as quickly as possible.

Web: www.redrapids.com

Email: support@redrapids.com

Phone: 972-671-9570

Fax: 972-671-9572

Please include the following information with your correspondence:

- Contact Information
- Product Model
- Host Card or System (PC, PCI Carrier, Single Board Computer)
- Operating System
- Problem Description