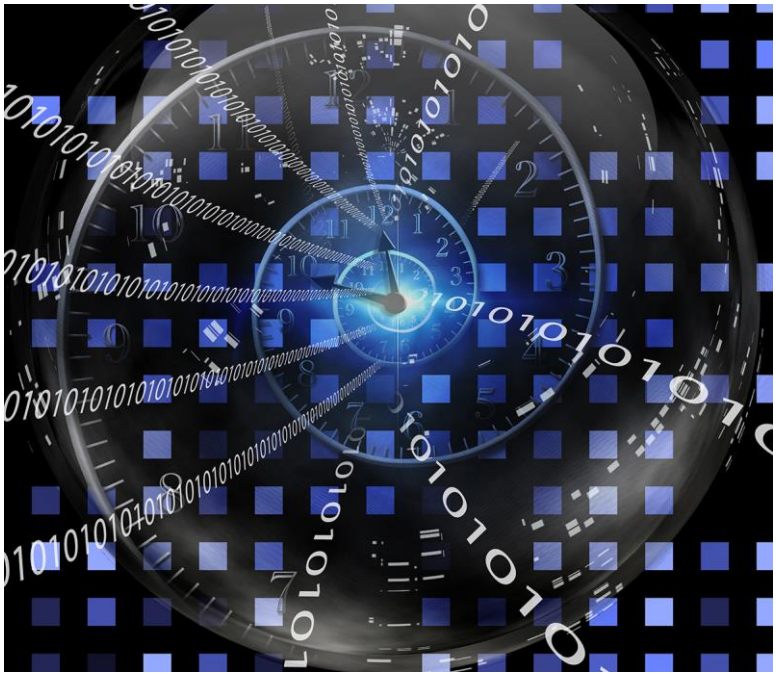
Event Scheduler Simplifies TDMA and Radar Processing



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Background

All Red Rapids signal acquisition and generation products offer multiple options to start and stop channel processing. The simplest control is a software command to capture a stream of digital samples from an analog-to-digital converter (ADC) or send a stream of samples to a digital-to-analog converter (DAC). A hardware trigger is also commonly used to synchronize channel processing with an external event.

Time division multiple access (TDMA) signals pose a specific challenge to general purpose hardware. These waveforms include a precision timing requirement beyond just starting and stopping the channel. Unique time slots are defined within a repeating frame so that a single frequency can service multiple subscribers. It is imperative that each subscriber remains confined to their assigned time slot to avoid interference.

Radars employ range gates that also rely on predefined time slots to collect return signals. The pulse repetition interval (PRI) may be divided into multiple gates that are delayed in time from the transmitted pulse.

The Red Rapids event scheduler allows precision timing of receiver or transmitter time slots encapsulated within a repeating frame. Up to 512 independent slots can be defined within the frame using the ADC or DAC sample clock as the time base.

Frame Duration

Defining the frame duration is the first step in setting up the event scheduler. The frame duration corresponds to a specified number of ADC sample clock periods in a receiver channel or DAC sample clock periods in a transmitter channel.

Figure 1 illustrates a 500 ms frame that is created for a channel operating at a sample rate of 250 MHz. The clock period counter resets at the end of each frame so that time slots within a frame are always referenced to zero.

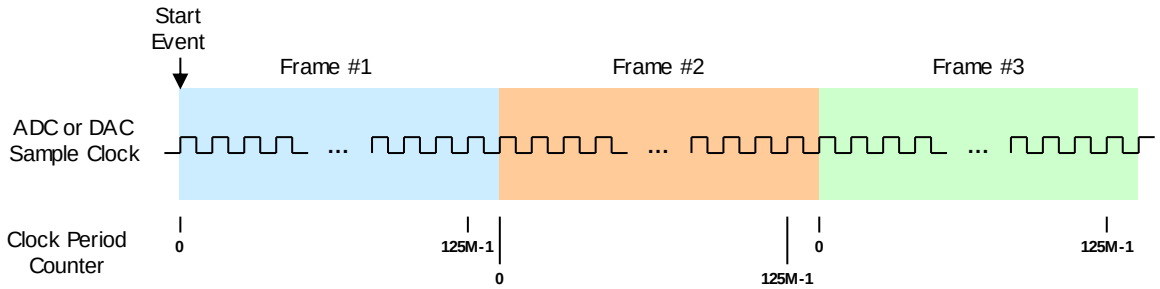

Figure 1 500 ms Frame Derived From 250 MHz Sample Clock

The first frame is activated by any start event available to the hardware. This could be a simple software command, an external trigger, or even a specific time of day. The channel will continue to process frames until the requested stop event is encountered. One option is to stop after a specified number of frames has been processed.

Time Slots

Each time slot within a frame is defined by a start time and a duration. Both are measured to the same sample clock period resolution used to define the frame duration. The start time for each slot is expressed as an offset from the start of each frame.

Figure 2 illustrates a simple example of a frame schedule that consists of two short time slots that occur very near the start of each frame. The first slot is scheduled to start three clock periods into the frame with a duration of six clock periods (3/6). The second slot starts fourteen clock periods into the frame with a duration of nine clock periods (14/9).

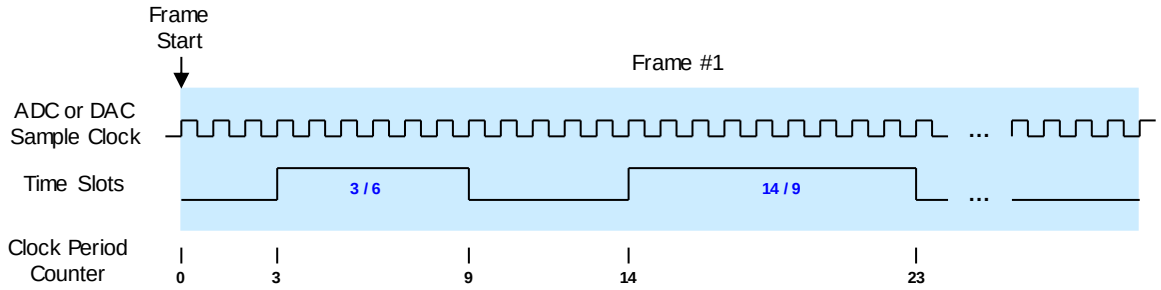

Figure 2 Two-Slot Timing Example

This example demonstrates the basic concept behind programming the scheduler, but it is not very realistic. A typical application would have much longer duration time slots spread throughout the entire frame as shown in Figure 3. This example demonstrates a five-slot schedule with a very high duty cycle. The figure also illustrates the repeating pattern within each frame.

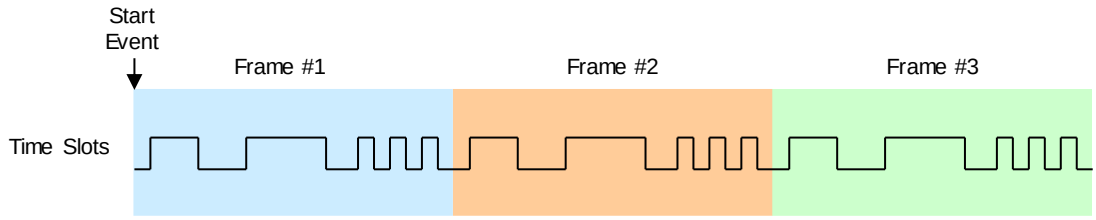

Figure 3 Five-Slot Schedule Example

Frame Descriptor File

The scheduler is loaded from a frame descriptor file that consists of alternating values to define the start time and duration of each slot. There can be up to 512 individual slots defined per frame. Figure 4 displays the contents of an example file that could be applied to the five-slot schedule shown in Figure 3. Keep in mind that each value is expressed in clock periods, so a complete frame would be 125 million clock periods in this example.

```
6250000   (slot start)
18750000  (slot duration)
43750000  (slot start)
31250000  (slot duration)
87500000  (slot start)
6250000   (slot duration)
100000000 (slot start)
6250000   (slot duration)
112500000 (slot start)
6250000   (slot duration)
```

Figure 4 Five-Slot Frame Descriptor File Example